ECC UDIMM

DDR5 5600

Datasheet

Products

TS2GLA72V6E

Product Description

16GB DDR5 5600 ECC-DIMM 1Rx8 2Gx8 CL46 1.1V

Datasheet version

1.0

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Revision History

Revision No.	History	Released Date	Editor by
1.0	First version	2023/11/08	PM

Transcend Features

Part Name	Capacity	Organization	Rank	Height	DIMM type	Note
TS2GLA72V6E	16GB	2Gx8	1	31.25mm	ECC UDIMM	Anti-sulfur

FEATURES

- Operating Temperature : 0°C to +95°C
- RoHS compliant products.
- VDD = VDDQ = 1.1V (1.067V(- 3%) ~ 1.166V(+6%))
- VPP = 1.8V(1.746V(-3%) ~ 1.908V(+6%))
- Clock Freq: 2800MHz for 5600Mb/s/Pin.
- Programmable CAS Latency: 22,26,28,30,32,36,40,42,46,50
- 16n bit pre-fetch
- Burst Length: 16 by default
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- Multi-purpose command (MPC)
- On-Die ECC
- SPD Hub with Thermal Sensor
- hPPR and sPPR are supported
- 30 u" PCB golden finger thickness
- Embedded Anti-sulfur resistor

Table of Content

1. Introduction

1.1 General Feature Information

Hardware Feature

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1.2 Product List

DIMM Type	Part Name	Capacity
ECC Unbuffered Long-DIMM	TS2GLA72V6E	16GB

1.3 Ordering Information

T S 2 G L A 7 2 V 6 E

1 2 3 4 5 6 7

1 – Transcend
2 – DRAM module capacity = 2GB x 8
3 – Long DIMM
4 – Module memory bus width
5 – Operation voltage 1.1V
6 – 5600
7 – 2Gx8

2. Product Specifications

2.1 Interface and Compliance

- DDR5 5600 Long DIMM with 72 Bits data width
- ECC Unbuffered Memory
- RoHS Compliance
- CE and UKCA Compliance

2.2 Supply Voltage

[Table 1] Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.4	V	1)
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1)
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1)
Storage temperature	T_{STG}	-55~+100	°C	1), 2)

Note:

1. Stresses greater than those listed in this table may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device.For the measurement conditions, refer to JESD51-2 standard.

[Table 2] Recommended AC & DC Operating Conditions

Parameter	Symbol	Rating			Unit	Note
		Min	Typ.	Max		
Device Supply Voltage	VDD	1.067(-3%)	1.1	1.166(+6%)	V	1), 2), 3)
Supply Voltage for I/O	VDDQ	1.067(-3%)	1.1	1.166(+6%)	V	1), 2), 3)
Core Power Voltage	VPP	1.746(-3%)	1.8	1.908(+6%)	V	3)

Note:

1. VDD must be within 66mV of VDDQ.
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball

2.3 IDD Specification Parameters and Table

[Table 3] IDD Specification Parameters –16GB, 2G x 72 Module (1 Rank x 8)

Parameters	Symbol	IDD Max.	IDDQ Max.	IPP Max.	Unit
Operating One Bank Active-Precharge Current	IDD0	423	243	162	mA
Precharge Standby Current	IDD2N	252	243	126	mA
Precharge Power-Down Current	IDD2P	594	252	126	mA
Active Standby Current	IDD3N	513	243	144	mA
Active Power-Down Current	IDD3P	297	153	144	mA
Operating Burst Read Current	IDD4R	1746	1440	189	mA
Operating Burst Write Current	IDD4W	1980	1413	162	mA
Burst Refresh Current	IDD5B	2313	243	729	mA
Self Refresh Current	IDD6N	576	54	243	mA
Operating Bank Interleave Read Current	IDD7	2826	1431	657	mA

Note:

1. IDD values are for full operating range of Voltage and Temperature
2. Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

2.4 Timing Parameters and Specifications

[Table 4] Timing Parameters and Specifications

Speed		DDR5-4800		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**		
Read command to first data	tAA	16	22.222	ns	
Activate to Read or Write command delay time	tRCD	16	-	ns	
Row Precharge Time	tRP	16	-	ns	
Activate to Precharge command period	tRAS	32	5x tREFI	ns	
Activate to Activate or Refresh command period	tRC	48	-	ns	
Clock Timing					
Average Clock Period	tCK(avg)	0.357	<0.384	ns	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(8nCK, 5ns)		nCK	
WRITE CAS_n to WRITE CAS_n com- mand delay for same bank group	tCCD_L_WR	max(32nCK, 20ns)		ns	
WRITE CAS_n to WRITE CAS_n com- mand delay for same bank group, sec- ond write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)		nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)		nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)		nCK	
Four activate window for 2KB page size	tFAW_2K	Max(40nCK, 16.640ns)		ns	
Four activate window for 1KB page size	tFAW_1K	Max(32nCK, 13.312ns)		ns	
Delay from start of internal write trans- action to internal read command for dif- ferent bank group	tWTR_S	Max(4nCK, 2.5ns)		ns	
Delay from start of internal write trans- action to internal read command for same bank group	tWTR_L	Max(16nCK, 10ns)		ns	
Delay from start of internal write trans- action to internal read with auto pre- charge command for same bank	tWTRA	tWR-tRTP		ns	
Internal READ Command to PRE- CHARGE Command delay	tRTP	Max(12nCK, 7.5ns)		ns	
PRECHARGE (PRE) to PRECHARGE(PRE) delay	tPPD	2		nCK(avg)	
WRITE recovery time	tWR	30	-	ns	

2.5 Serial Presence Detect Specification

[Table 5] Serial Presence Detect Specification

TS2GLA72V6E Serial Presence Detect		
Byte No.	**Description**	**Hex Value**
0	Number of Bytes in SPD Device	30
1	SPD Revision	10
2	Host Bus Command Protocol Type	12
3	Module Type	02
4	First SDRAM Density and Package	04
5	First SDRAM Addressing	00
6	First SDRAM I/O Width	20
7	First SDRAM Bank Groups & Banks Per Bank Group	62
8	Second SDRAM Density and Package	00
9	Second SDRAM Addressing	00
10	Secondary SDRAM I/O Width	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	00
12	SDRAM BL32 & Post Package Repair	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	02
14	SDRAM Fault Handling and Temperature Sense	00
15	Reserved	00
16	SDRAM Nominal Voltage, VDD	00
17	SDRAM Nominal Voltage, VDDQ	00
18	SDRAM Nominal Voltage, VPP	00

19	SDRAM Timing	00
20	SDRAM Minimum Cycle Time(LSB)	65
21	SDRAM Minimum Cycle Time(MSB)	01
22	SDRAM Maximum Cycle Time(LSB)	F2
23	SDRAM Maximum Cycle Time(MSB)	03
24	SDRAM CAS Latencies Supported	7A
25		AD
26		00
27		00
28		00
29	Reserved	00
30-31	SDRAM Minimum CAS Latency Time (tAAmin)	80
		3E
32-33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin)	80
		3E
34-35	SDRAM Minimum Row Precharge Delay Time (tRPmin)	80
		3E
36-37	SDRAM Minimum Active to Precharge Delay Time (tRASmin)	00
		7D
38-39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin)	80
		BB
40-41	SDRAM Minimum Write Recovery Time (tWRmin)	30
		75
42-43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min)	27
		01
44-45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min)	A0
		00
46-47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin)	82
		00
48-49	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFC1min)	00
		00
50-51	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFC2min)	00
		00
52-53	SDRAM Minimum Refresh Recovery Delay Time,3DS Different Logical Rank (tRFCsbmin)	00
		00
54	SDRAM Refresh Management, First Byte, First SDRAM 1	00
55	SDRAM Refresh Management, Second Byte, First SDRAM 1	00

56	SDRAM Refresh Management, First Byte, Second SDRAM 1	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM 1	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM 1	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM 1	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM 1	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM 1	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM 1	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM 1	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM 1	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM 1	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM 1	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM 1	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM 1	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM 1	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (tRRD_Lmin)	88
71		13
72		08
73	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group (tCCD_Lmin)	88
74		13
75		08
76	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group (tCCD_L_WRmin)	20
77		4E
78		20
79	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group (tCCD_L_WR2min)	10
80		27
81		10
82	SDRAM Minimum Four Activate Window (tFAWmin)	A4
83		2C
84		20
85	SDRAM Minimum Write to Read Command Delay Time,	10

86	Same Bank Group (tCCD_L_WTRmin)	27
87		10
88	SDRAM Minimum Write to Read Command Delay Time, Different Bank Group(tCCD_S_WTRmin)	C4
89		09
90		04
91	SDRAM Minimum Read to Precharge Command Delay Time, (tRTPmin)	4C
92		1D
93		0C
94-127	Base Configuration Section	00
128-191	Reserved for future use	00
192	SPD Revision for SPD bytes 192~447	10
193	Hashing Sequence	00
194	SPD Manufacturer ID Code, First Byte	Variable
195	SPD Manufacturer ID Code, Second Byte	Variable
196	SPD Device Type	Variable
197	SPD Device Revision Number	Variable
198	PMIC 0 Manufacturer ID Code, First Byte	Variable
199	PMIC 0 Manufacturer ID Code, Second Byte	Variable
200	PMIC 0 Device Type	Variable
201	PMIC 0 Revision Number	Variable
202	PMIC 1 Manufacturer ID Code, First Byte	Variable
203	PMIC 1 Manufacturer ID Code, Second Byte	Variable
204	PMIC 1 Device Type	Variable
205	PMIC 1 Revision Number	Variable
206	PMIC 2 Manufacturer ID Code, First Byte	Variable
207	PMIC 2 Manufacturer ID Code, Second Byte	Variable
208	PMIC 2 Device Type	Variable
209	PMIC 2 Revision Number	Variable
210	Thermal Sensor Manufacturer ID Code, First Byte	Variable
211	Thermal Sensor Manufacturer ID Code, Second Byte	Variable
212	Thermal Sensor Device Type	Variable
213	Thermal Sensor Revision Number	Variable
214-229	Reserved	00
230	Module Nominal Height	11
231	Module Maximum Thickness	01
232	Reference Raw Card Used	03
233	DIMM Attributes	81
234	Module Organization	00
235	Memory Channel Bus Width	2A

236-239	Reserved	00
240-447	Reserved	00
448-509	Reserved for future use	00
510-511	CRC for bytes 0-509	Variable
512	Module Manufacturer's ID Code	01
513		4F
514	Module Manufacturing Location	54
515	Module Manufacturing Date	Variable
516		Variable
517-520	Module Serial Number	Variable
521-550	Module Part Number	Note 1
551	Module Revision Code	00
552	DRAM Manufacturer ID Code	Variable
553		Variable
554	DRAM Stepping	Variable
555-639	Manufacturer's Specific Data	Variable
640-1023	End User Programmable	Variable

Note:

1. The detail Model Part Number is listed as below.

Byte	521	522	523	524	525	526	527	528	529	530	531	532	533	534
PN	T	S	2	G	L	A	7	2	V	6	E			
Hex	54	53	32	47	4C	41	37	32	56	36	45	20	20	20

Byte	535	536	537	538	539	540	541	542	543	544	545	546	547	548
PN														
Hex	20	20	20	20	20	20	20	20	20	20	20	20	20	20

Byte	549	550
PN		
Hex	20	20

2.6 Hub Device Address

[Table 6] Hub Device Address

	Local Device Type ID (LID)					Host ID (HID)	HSA Pin connection
	PMIC	SPD Hub	RCD	TS0	TS1		
DIMM 0	1001	1010	1011	0010	0110	000	10.0 KΩ to GND
DIMM 1	1001	1010	1011	0010	0110	001	15.4 KΩ to GND
DIMM 2	1001	1010	1011	0010	0110	010	23.2 KΩ to GND
DIMM 3	1001	1010	1011	0010	0110	011	35.7 KΩ to GND
DIMM 4	1001	1010	1011	0010	0110	100	54.9 KΩ to GND
DIMM 5	1001	1010	1011	0010	0110	101	84.5 KΩ to GND
DIMM 6	1001	1010	1011	0010	0110	110	127 KΩ to GND
DIMM 7	1001	1010	1011	0010	0110	111	196 KΩ to GND

Note:

1. RCD/TS0/TS1 is not used on Unbufferd DIMM

2.7 SPD HUB & PMIC Operating Conditions

[Table 7] SPD HUB operating conditions

Parameter	Symbol	Min	Typ	Max	Units
Input Supply Voltage	V_{DDSPD}	1.7	1.8	1.98	V
Input Supply Voltage	V_{DDIO}	0.95	1	1.05	V
Case operating temperature	T_{CASE}	-40		125	°C
Case temperature range for NVM Write operation Data writes outside this range may not meet retention requirements.	$T_{WRITEOK}$	-40		95	°C

[Table 8] PMIC operating conditions

Parameter	Symbol	Min	Typ	Max	Units	note
Bulk Input Supply Voltage	VIN_Bulk	4.25	5	5.5	V	1)
Maximum Input Current for VIN_Bulk	IVIN_Bulk	0.05	-	2	A	2)

Note:

1. During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply.
2. The minimum input current requirement is to deliver the maximum output current on VOUT_1.8V and VOUT_1.0V LDO plus the current required by the PMIC for its own use. The maximum input current PMIC may see on its all VIN_Bulk input.

2.8 Environment Specifications

[Table 9] Operating Temperature condition

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	DRAM Operating Temperature	0 to 95	°C	1),2),3)
T_{STG}	Storage Temperature	-55 to 100	°C	4)

Note:

1. Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values. See JESD402-1 for details.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. Average Refresh Period 3.9us at lower than Tcase 85°C , 1.95us at 85°C < Tcase ≤ 95°C. For more details, please refer to JESD79-5.
4. Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

2.9 System Reliability

[Table 10] Telcordia SR332 issue 4 MTBF Specifications

Parameter	TS2GLA72V6E
MTBF	> 1,500,000 hours

Note:

1. The calculation is based on 25°C.

[Table 11] Warranty

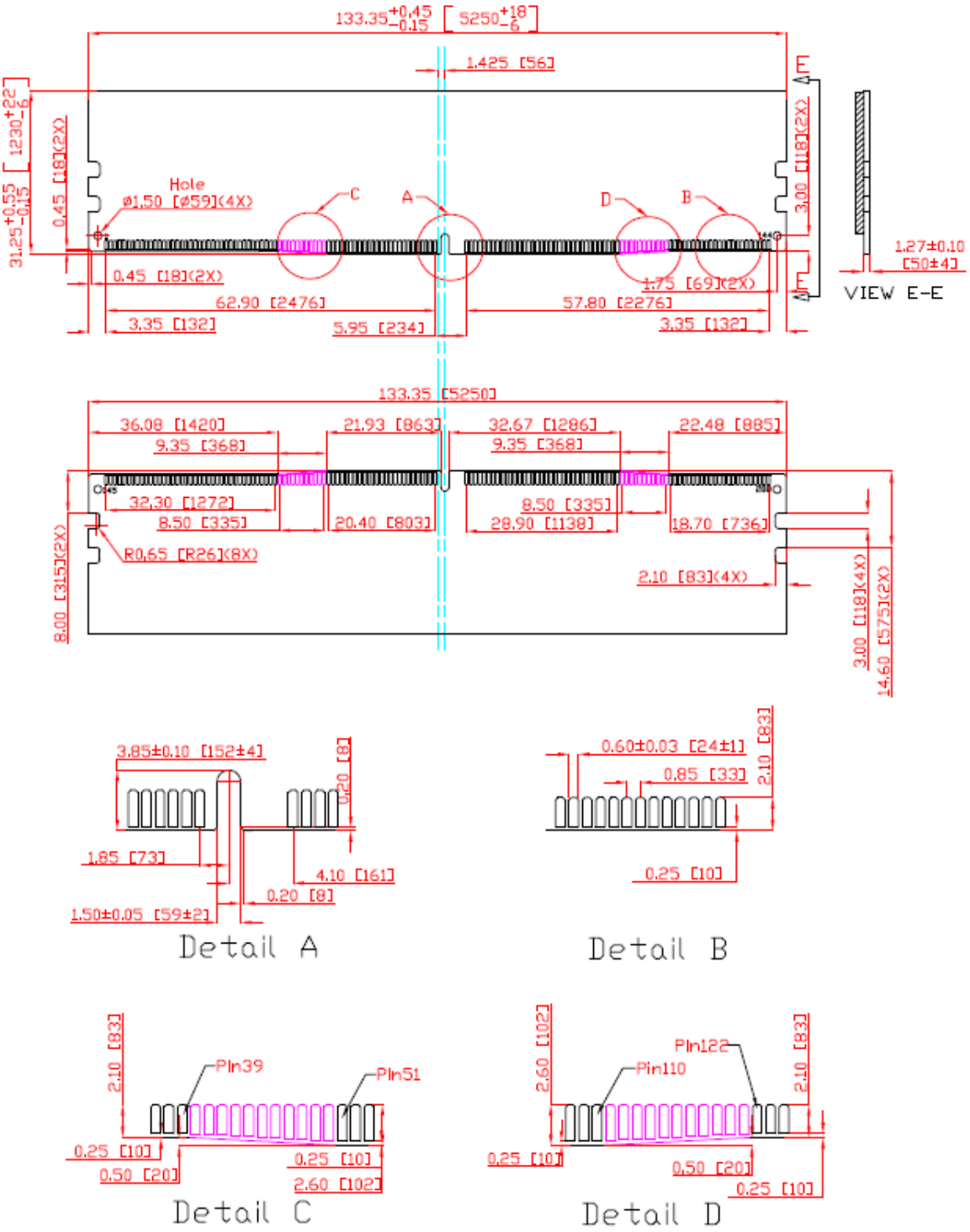
Parameter	TS2GLA72V6E
Warranty	Limited Lifetime Warranty

3. Mechanical Specification

The figure below illustrates the Transcend DDR5 ECC Long DIMM.

[Table 12] Physical Dimensions and Weight

Model	Thickness (mm)	Width (mm)	Length (mm)	Weight (gram)
TS2GLA72V6E	Max 2.67	133.35	31.25	NA



Note : All dimensions are in millimeters[mils] and should be kept within a tolerance of ±0.15[6], unless otherwise specified.

4. Pin Assignments

4.1 Pin Assignments

[Table 13] Pin Assignments

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	145	VIN_BULK	75	RFU	219	RFU
2	RFU	146	VIN_BULK	KEY			
3	RFU	147	PWR_GOOD	76	RFU	220	RFU
4	HSCL	148	HSA	77	VSS	221	VSS
5	HSDA	149	RFU	78	CK0_B_t	222	CK1_B_t
6	VSS	150	VSS	79	CK0_B_c	223	CK1_B_c
7	RFU	151	PWR_EN	80	VSS	224	VSS
8	VSS	152	RFU	81	RFU	225	RFU
9	DQ0_A	153	VSS	82	CA12_B	226	RFU
10	VSS	154	DQ2_A	83	VSS	227	VSS
11	DQ1_A	155	VSS	84	CA10_B	228	CA11_B
12	VSS	156	DQ3_A	85	CA8_B	229	CA9_B
13	DQS0_A_c	157	VSS	86	VSS	230	VSS
14	DQS0_A_t	158	DM0_A_n	87	CA6_B	231	CA7_B
15	VSS	159	VSS	88	CA4_B	232	CA5_B
16	DQ4_A	160	DQ6_A	89	VSS	233	VSS
17	VSS	161	VSS	90	CA2_B	234	CA3_B
18	DQ5_A	162	DQ7_A	91	CA0_B	235	CA1_B
19	VSS	163	VSS	92	VSS	236	VSS
20	DQ8_A	164	DQ10_A	93	CS0_B_n	237	CS1_B_n
21	VSS	165	VSS	94	VSS	238	VSS
22	DQ9_A	166	DQ11_A	95	RESET_n	239	DQS4_B_c
23	VSS	167	VSS	96	VSS	240	DQS4_B_t
24	DM1_A_n	168	DQS1_A_c	97	CB0_B	241	VSS
25	VSS	169	DQS1_A_t	98	VSS	242	CB2_B
26	DQ12_A	170	VSS	99	CB1_B	243	VSS
27	VSS	171	DQ14_A	100	VSS	244	CB3_B
28	DQ13_A	172	VSS	101	DQ0_B	245	VSS
29	VSS	173	DQ15_A	102	VSS	246	DQ2_B
30	DQ16_A	174	VSS	103	DQ1_B	247	VSS
31	VSS	175	DQ18_A	104	VSS	248	DQ3_B
32	DQ17_A	176	VSS	105	DQS0_B_c	249	VSS
33	VSS	177	DQ19_A	106	DQS0_B_t	250	DM0_B_n
34	DQS2_A_c	178	VSS	107	VSS	251	VSS
35	DQS2_A_t	179	DM2_A_n	108	DQ4_B	252	DQ6_B
36	VSS	180	VSS	109	VSS	253	VSS

37	DQ20_A	181	DQ22_A	110	DQ5_B	254	DQ7_B
38	VSS	182	VSS	111	VSS	255	VSS
39	DQ21_A	183	DQ23_A	112	DQ8_B	256	DQ10_B
40	VSS	184	VSS	113	VSS	257	VSS
41	DQ24_A	185	DQ26_A	114	DQ9_B	258	DQ11_B
42	VSS	186	VSS	115	VSS	259	VSS
43	DQ25_A	187	DQ27_A	116	DM1_B_n	260	DQS1_B_c
44	VSS	188	VSS	117	VSS	261	DQS1_B_t
45	DM3_A_n	189	DQS3_A_c	118	DQ12_B	262	VSS
46	VSS	190	DQS3_A_t	119	VSS	263	DQ14_B
47	DQ28_A	191	VSS	120	DQ13_B	264	VSS
48	VSS	192	DQ30_A	121	VSS	265	DQ15_B
49	DQ29_A	193	VSS	122	DQ16_B	266	VSS
50	VSS	194	DQ31_A	123	VSS	267	DQ18_B
51	CB0_A	195	VSS	124	DQ17_B	268	VSS
52	VSS	196	CB2_A	125	VSS	269	DQ19_B
53	CB1_A	197	VSS	126	DQS2_B_c	270	VSS
54	VSS	198	CB3_A	127	DQS2_B_t	271	DM2_B_n
55	DQS4_A_c	199	VSS	128	VSS	272	VSS
56	DQS4_A_t	200	ALERT_n	129	DQ20_B	273	DQ22_B
57	VSS	201	VSS	130	VSS	274	VSS
58	CS0_A_n	202	CS1_A_n	131	DQ21_B	275	DQ23_B
59	VSS	203	VSS	132	VSS	276	VSS
60	CA0_A	204	CA1_A	133	DQ24_B	277	DQ26_B
61	CA2_A	205	CA3_A	134	VSS	278	VSS
62	VSS	206	VSS	135	DQ25_B	279	DQ27_B
63	CA4_A	207	CA5_A	136	VSS	280	VSS
64	CA6_A	208	CA7_A	137	DM3_B_n	281	DQS3_B_c
65	VSS	209	VSS	138	VSS	282	DQS3_B_t
66	CA8_A	210	CA9_A	139	DQ28_B	283	VSS
67	CA10_A	211	CA11_A	140	VSS	284	DQ30_B
68	VSS	212	VSS	141	DQ29_B	285	VSS
69	CA12_A	213	RFU	142	VSS	286	DQ31_B
70	RFU	214	RFU	143	RFU	287	VSS
71	VSS	215	VSS	144	RFU	288	RFU
72	CK0_A_t	216	CK1_A_t				
73	CK0_A_c	217	CK1_A_c				
74	VSS	218	VSS				

4.2 Pin Description

[Table 14] Pin Description

Symbol	Type	I/O Level	Function
CK0_A_t, CK0_A_c CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c CK1_B_t, CK1_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B –CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n – CS1_A_n CS0_B_n – CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A – DQ31_A DQ0_B – DQ31_B	Input/Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode Register, then CRC code is added at the end of Data Burst.
CB0_A – CB3_A CB0_B – CB3_B	Input/Output	VDDQ	DIMM ECC check bits
DQS0_A_t – DQS4_A_t DQS0_A_c – DQS4_A_c DQS0_B_t – DQS4_B_t DQS0_B_c – DQS4_B_c	Input/Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n – DM3_A_n DM0_B_n – DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.

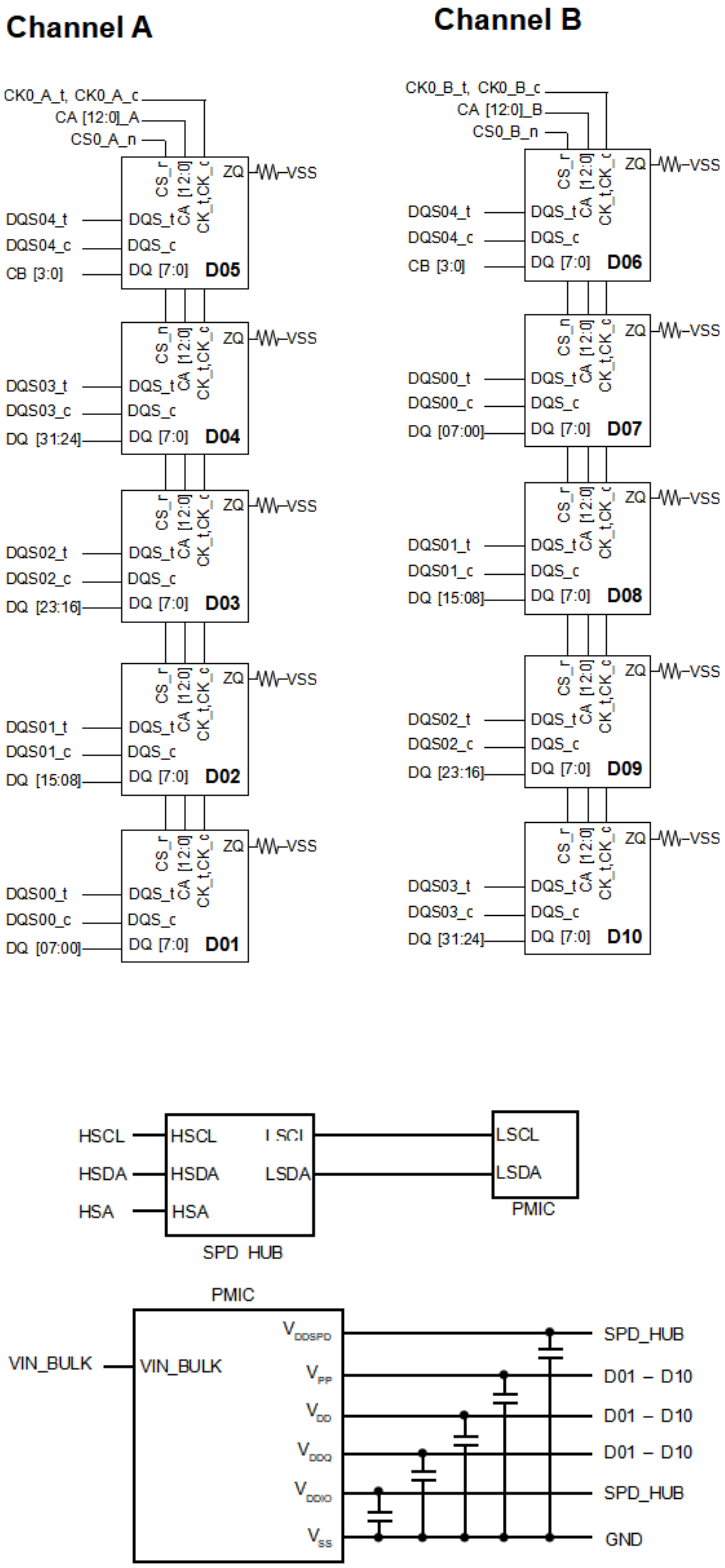
Symbol	Type	I/O Level	Function
ALERT_n	Input/Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input.Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input/Output	1.0V	Host SidebandBus data, connected from the controller to Hubs or Host bus Target devices.
HSA	Input	2.1V	Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic address range.
RFU	Reserved for future use		Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input/Output	Open Drain	Power good indicator. Open Drain output.
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5V	5 V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

Pin Name	Description	Pin Name	Description
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes(negative line of differential pair)	VIN_BULK	5 V power input supply to the PMIC for analog circuits
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus	HSCL	SidebandBus clock
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select	HSDA	SidebandBus data
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus	HSA	SidebandBus address
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B			

5. Block Diagram

5.1 Block Diagram

16GB, 2G x 72 Module (1 Rank x 8) TS2GLA72V6E



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