**MMS4X00-NS400-AO**

Mellanox® MMS4X00-NS400 Compatible TAA 400GBase-DR4 PAM4 OSFP112 RHS Transceiver (SMF, 1310nm, 500m, MPO, DOM, CMIS 5.0)

**Features**

- 4x100G PAM4 Data Rates
- Hot Pluggable OSFP Form Factor
- Single 3.3V Power Supply
- I2C Management Interface Compliant to CMIS Rev5.0
- Compliant with IEEE 802.3 bs 400GBASE-DR4
- Electrical Interface Compliant with 100Gbps Per Lane Defined by IEEE 802.3ck
- Internal CDR on Both Transmitter and Receiver Channels
- PIN Receiver
- Operating Temperature: 0 to 70 Celsius
- Cooled 1310nm EML Laser
- RoHS Compliant and Lead-Free

**Applications**

- 400GBase Ethernet

**Product Description**

This Mellanox® MMS4X00-NS400 compatible OSFP112 RHS transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is guaranteed to be 100% compatible with the equivalent Mellanox® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Maximum Supply Voltage | Vcc | -0.5 | | 3.6 | V |
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Storage Temperature | Tstg | -40 | | 85 | °C |
| Operating Temperature | Tc | 0 | 40 | 70 | °C |
| Relative Humidity | RH | 15 | | 85 | % |
| Data Rate | | | 106.25±100ppm | | Gbps |

**Notes:**

1. Stressed in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the datasheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

## Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Module Supply Current | Icc | | | 2.87 | A | |
| Power Dissipation | $P_{DISS}$ | | | 9 | W | |
| **Transmitter** | | | | | | |
| Input Differential Impedance | ZIN | 90 | 100 | 110 | Ω | |
| Differential Data Input Swing | VIN,pp | | | 900 | mVp-p | |
| DC Common-Mode Input Voltage | | -350 | | 2850 | mV | |
| **Receiver** | | | | | | |
| Output Differential Impedance | ZOUT | 90 | 100 | 110 | Ω | |
| Differential Data Output Swing | VOUT,pp | | | 900 | mVp-p | 1 |
| **Dual Function Signals** | | | | | | |
| INT/RSTn | V_INT/RSTn_1 | 0.000 | 0.000 | 1.000 | V | 2 |
| | V_INT/RSTn_2 | 0.000 | 0.000 | 1.000 | V | 3 |
| | V_INT/RSTn_3 | 1.500 | 1.900 | 2.250 | V | 4 |
| | V_INT/RSTn_4 | 2.750 | 3.000 | 3.465 | V | 5 |
| LPWn/PRSn | V_LPWn/PRSn_1 | 0.000 | 0.950 | 1.100 | V | 6 |
| | V_LPWn/PRSn_2 | 1.400 | 1.700 | 2.250 | V | 7 |
| | V_LPWn/PRSn_3 | 2.750 | 3.300 | 3.465 | V | 8 |

**Notes:**

1. Internally AC coupled but requires an external 100Ω differential load termination.
2. INT/RSTn voltage for no Module.

3. INT/RSTn voltage for Module installed, H_RSTn=Low.
4. INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low.
5. INT/RSTn voltage for Module installed, H_RSTn=High, M_INT= High.
6. LPWn/PRSn voltage for Module installed, H_LPWn=Low.
7. LPWn/PRSn voltage for Module installed, H_LPWn =High.
8. LPWn/PRSn voltage for no Module.

## Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| **Average Launch Power Per Lane** | Pavg | -2.9 | | 4 | dBm | 1 |
| **Outer Optical Modulation Amplitude Per Lane** | POMA | -0.8 | | 4.2 | dBm | 1 |
| **Extinction Ratio** | ER | 3.5 | | | dB | |
| **Lane Wavelengths** | λ | 1304.5 | | 1317.5 | nm | |
| **Side-Mode Suppression Ratio** | SMSR | 30 | | | dB | |
| **Transmitter and Dispersion Penalty Eye Closure Per Lane** | TDECQ | | | 3.4 | dB | |
| **Launch Power in OMAouter Minus TDECQ Per Lane** | OMA-TDECQ | -2.2 | | | dBm | |
| **Average Launch Power of Off Transmitter** | Poff | | | -15 | dBm | |
| **Optical Return Loss Tolerance** | ORLT | | | 21.4 | dB | |
| **Transmitter Reflectance** | | | | -26 | dB | |
| **Receiver** | | | | | | |
| **Lane Wavelengths** | λ | 1304.5 | | 1317.5 | nm | |
| **Receiver Sensitivity (OMA)** | RxSENS | | | -3.9 | dBm | 2 |
| **Receiver Overload Per Lane (Pavg)** | POL | 4 | | | dBm | |
| **Damage Threshold Per Lane** | | 5 | | | dBm | |
| **Receiver Power Per Lane (OMAouter)** | OMA | | | 4.2 | dBm | |
| **Receiver Reflectance** | | | | -26 | dB | |
| **LOS De-Assert** | LOSD | | | -10 | dBm | |
| **LOS Assert** | LOSA | -16 | | | dBm | |
| **LOS Hysteresis** | | 0.5 | | | dB | |

**Notes:**
1. Class 1 Laser Safety per FDA/CDRH and EN (IEC) 60825 regulations.
2. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, and BER<$2.4E^{-4}$.

## Pin Descriptions

| Pin | Logic | Symbol | Name/Description | Direction | Plug Sequence | Notes |
|-----|-------|--------|------------------|-----------|---------------|-------|
| 1 | | GND | Module Ground. | | 1 | |
| 2 | CML-I | Tx2+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 3 | CML-I | Tx2- | Transmitter Inverted Data. | Input from Host | 3 | |
| 4 | | GND | Module Ground. | | 1 | |
| 5 | CML-I | Tx4+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 6 | CML-I | Tx4- | Transmitter Inverted Data. | Input from Host | 3 | |
| 7 | | GND | Module Ground. | | 1 | |
| 8 | CML-I | Tx6+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 9 | CML-I | Tx6- | Transmitter Inverted Data. | Input from Host | 3 | |
| 10 | | GND | Module Ground. | | 1 | |
| 11 | CML-I | Tx8+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 12 | CML-I | Tx8- | Transmitter Inverted Data. | Input from Host | 3 | |
| 13 | | GND | Module Ground. | | 1 | |
| 14 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock. | Bi-Directional | 3 | 1 |
| 15 | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| 16 | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| 17 | Multi-Level | LPWn/PRSn | Low-Power Mode/Module Present. | Bi-Directional | 3 | 2 |
| 18 | | GND | Module Ground. | | 1 | |
| 19 | CML-O | Rx7- | Receiver Inverted Data. | Output to Host | 3 | |
| 20 | CML-O | Rx7+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 21 | | GND | Module Ground. | | 1 | |
| 22 | CML-O | Rx5- | Receiver Inverted Data. | Output to Host | 3 | |
| 23 | CML-O | Rx5+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 24 | | GND | Module Ground. | | 1 | |
| 25 | CML-O | Rx3- | Receiver Inverted Data. | Output to Host | 3 | |
| 26 | CML-O | Rx3+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 27 | | GND | Module Ground. | | 1 | |
| 28 | CML-O | Rx1- | Receiver Inverted Data. | Output to Host | 3 | |
| 29 | CML-O | Rx1+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 30 | | GND | Module Ground. | | 1 | |
| 31 | | GND | Module Ground. | | 1 | |
| 32 | CML-O | Rx2+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 33 | CML-O | Rx2- | Receiver Inverted Data. | Output to Host | 3 | |
| 34 | | GND | Module Ground. | | 1 | |
| 35 | CML-O | Rx4+ | Receiver Non-Inverted Data. | Output to Host | 3 | |

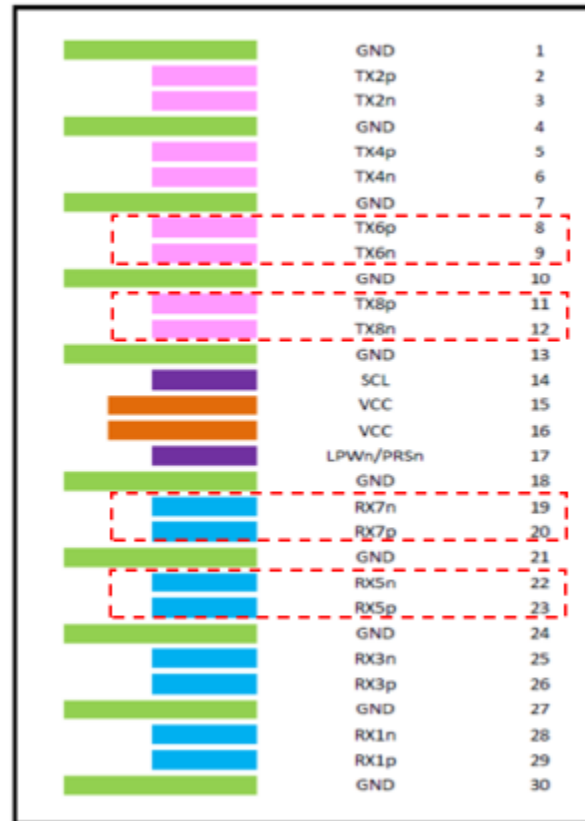| 36 | CML-O | Rx4- | Receiver Inverted Data. | Output to Host | 3 | |
| 37 | | GND | Module Ground. | | 1 | |
| 38 | CML-O | Rx6+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 39 | CML-O | Rx6- | Receiver Inverted Data. | Output to Host | 3 | |
| 40 | | GND | Module Ground. | | 1 | |
| 41 | CML-O | Rx8+ | Receiver Non-Inverted Data. | Output to Host | 3 | |
| 42 | CML-O | Rx8- | Receiver Inverted Data. | Output to Host | 3 | |
| 43 | | GND | Module Ground. | | 1 | |
| 44 | Multi-Level | INT/RSTn | Module Interrupt/Module Reset. | Bi-Directional | 3 | 2 |
| 45 | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| 46 | | Vcc | +3.3V Power Supply. | Power from Host | 2 | |
| 47 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data. | Bi-Directional | 3 | 1 |
| 48 | | GND | Module Ground. | | 1 | |
| 49 | CML-I | Tx7- | Transmitter Inverted Data. | Input from Host | 3 | |
| 50 | CML-I | Tx7+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 51 | | GND | Module Ground. | | 1 | |
| 52 | CML-I | Tx5- | Transmitter Inverted Data. | Input from Host | 3 | |
| 53 | CML-I | Tx5+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 54 | | GND | Module Ground. | | 1 | |
| 55 | CML-I | Tx3- | Transmitter Inverted Data. | Input from Host | 3 | |
| 56 | CML-I | Tx3+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 57 | | GND | Module Ground. | | 1 | |
| 58 | CML-I | Tx1- | Transmitter Inverted Data. | Input from Host | 3 | |
| 59 | CML-I | Tx1+ | Transmitter Non-Inverted Data. | Input from Host | 3 | |
| 60 | | GND | Module Ground. | | 1 | |

**Notes:**

1. Open-drain with pull-up resistor on the host.
2. See pin description of OSFP MSA for required circuit.
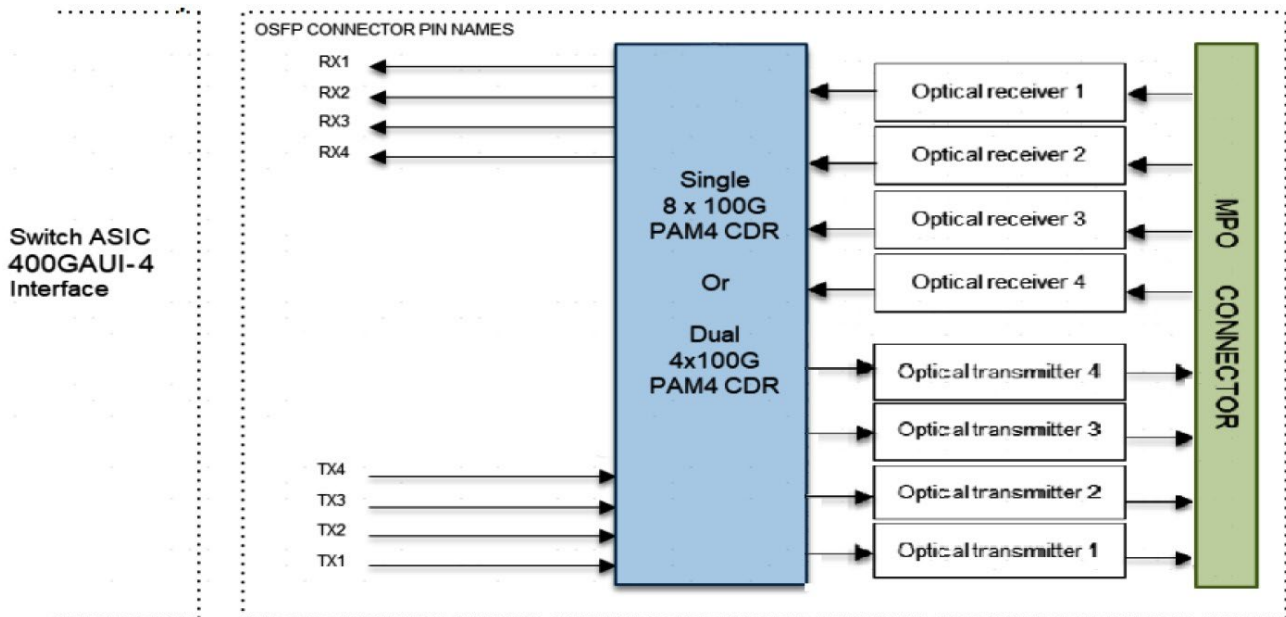
**Electrical Pad Layout**

## Top Side (viewed from top)

| Pin | Name |
|-----|------|
| 60 | GND |
| 59 | TX1p |
| 58 | TX1n |
| 57 | GND |
| 56 | TX3p |
| 55 | TX3n |
| 54 | GND |
| 53 | TX5p |
| 52 | TX5n |
| 51 | GND |
| 50 | TX7p |
| 49 | TX7n |
| 48 | GND |
| 47 | SDA |
| 46 | VCC |
| 45 | VCC |
| 44 | INT/RSTn |
| 43 | GND |
| 42 | RX8n |
| 41 | RX8p |
| 40 | GND |
| 39 | RX6n |
| 38 | RX6p |
| 37 | GND |
| 36 | RX4n |
| 35 | RX4p |
| 34 | GND |
| 33 | RX2n |
| 32 | RX2p |
| 31 | GND |

---- Module Card Edge ----

## Bottom Side (viewed from bottom)

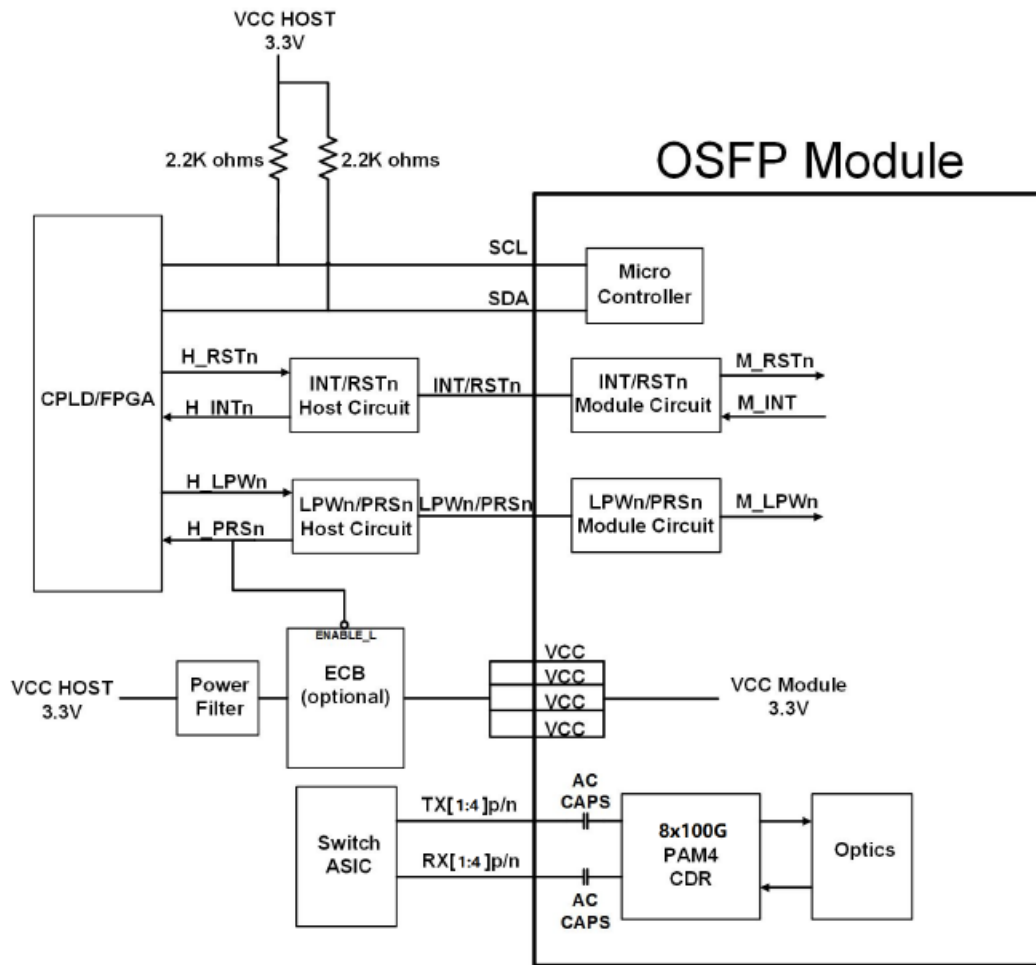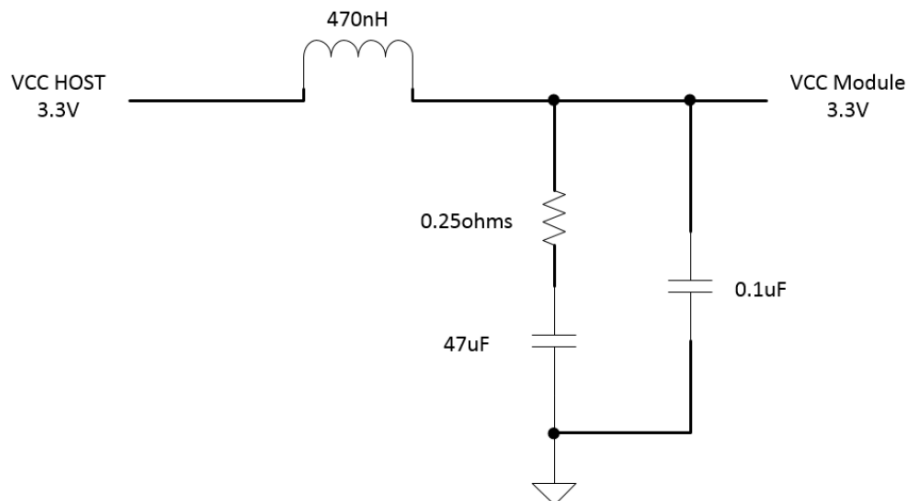| Name | Pin |
|------|-----|
| GND | 1 |
| TX2p | 2 |
| TX2n | 3 |
| GND | 4 |
| TX4p | 5 |
| TX4n | 6 |
| GND | 7 |
| TX6p | 8 |
| TX6n | 9 |
| GND | 10 |
| TX8p | 11 |
| TX8n | 12 |
| GND | 13 |
| SCL | 14 |
| VCC | 15 |
| VCC | 16 |
| LPWn/PRSn | 17 |
| GND | 18 |
| RX7n | 19 |
| RX7p | 20 |
| GND | 21 |
| RX5n | 22 |
| RX5p | 23 |
| GND | 24 |
| RX3n | 25 |
| RX3p | 26 |
| GND | 27 |
| RX1n | 28 |
| RX1p | 29 |
| GND | 30 |

**Block Diagram**

## Recommended Application Interface Block Diagram



## Recommended Host Board Power Supply Filter Network

**About AddOn Networks**

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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